NOTRE DAME UNIVERSITY BANGLADESH

VLSI Design Lab Report-03

Course Code: CSE-4218
Course Title: VLSI Design Lab
Experiment Name: Implementing Adder Circuit

Submitted by:

Name: Istiak Alam
ID: 0692230005101005
Batch: CSE-20

Submission Date: April 30, 2026

Submitted to:

Nfisa Tabassum,
Lecturer, Dept. of CSE
Notre Dame University Bangladesh

Table of Contents

Abstract

This laboratory experiment presents the design and implementation of Adder Circuit using the DSCH2 schematic simulation tool. The circuits were designed following standard CMOS pull-up and pull-down network principles. For each logic function, the corresponding truth table was derived and verified through schematic simulation. Timing diagrams were analyzed to observe the dynamic response and switching behavior of the circuits. The experimental results confirm that the implemented CMOS designs satisfy the expected logical and temporal characteristics of the half adder circuit.

1 Introduction

A combinational logic circuit which is designed to add two binary digits is called as a half adder. The half adder provides the output along with a carry value (if any). The half adder circuit is designed by connecting an EX-OR gate and one AND gate. It has two input terminals and two output terminals for sum and carry.

2 Objective

The objectives of this VLSI-Lab experiment are as follows:

- To implement Adder Circuit using CMOS logic design methodology.
- To design schematic-level Adder circuits using the DSCH2 tool.
- To verify the logical correctness of the implemented circuits using truth tables.
- To analyze timing diagrams to observe signal transitions and propagation behavior.
- To develop a clear understanding of Adder Circuit.

3 Half Adder Function

3.1 Boolean Function

$$Sum = AB' + A'B$$

$$Carry = A\ B$$

3.2 Truth Table

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3.3 Schematic Image

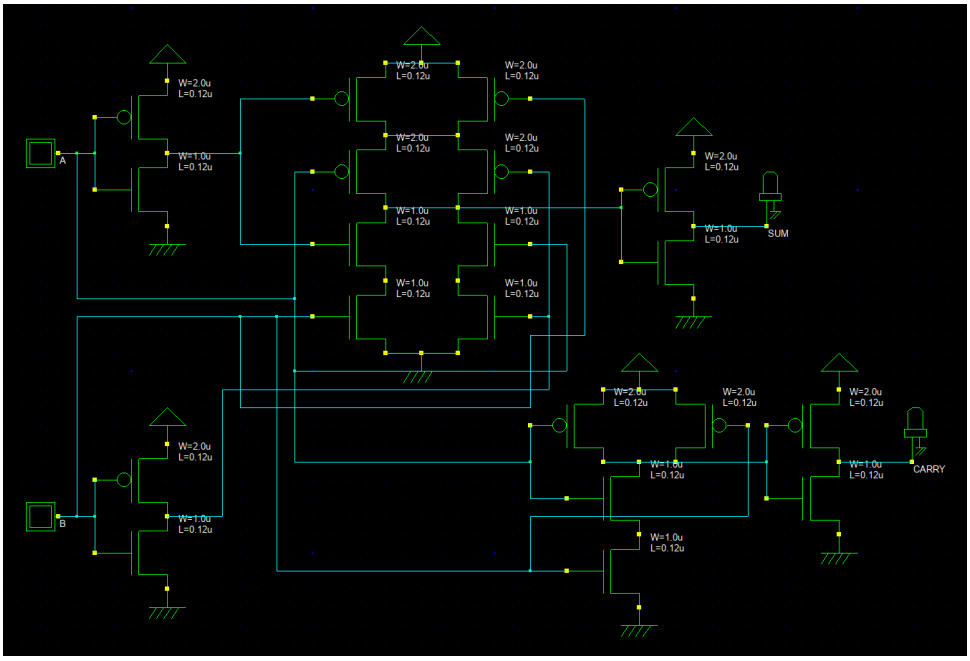

Figure 1: CMOS Schematic of Half-Adder

3.4 Timing Diagram

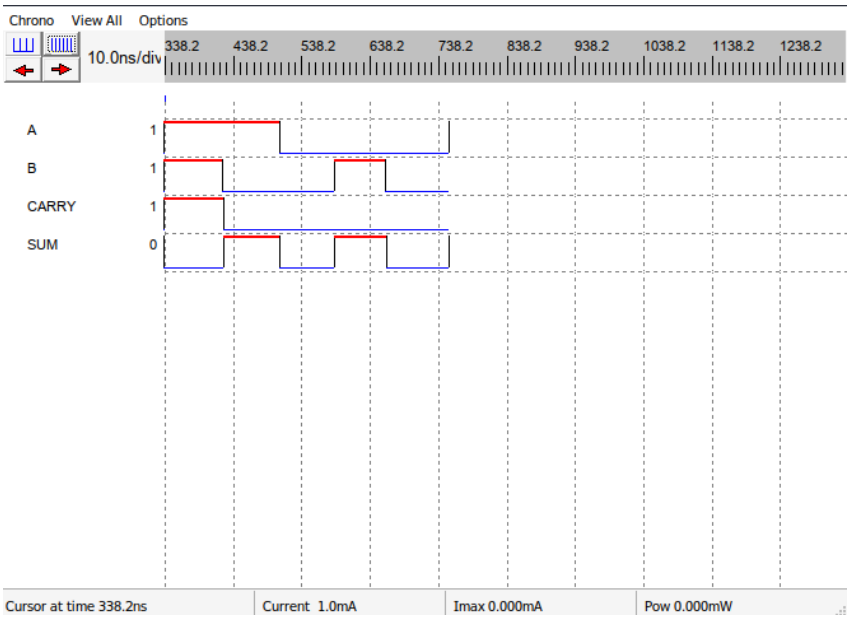

Figure 2: Timing Diagram of Half-Adder

3.5 Observation

The timing diagram of a half adder illustrates the sequence of operations that occur when two binary inputs are added. The diagram typically shows the timing of the XOR opera-

tion for the sum and the timing of the AND operation for the carry. The timing diagram can help in understanding the propagation delay and the timing constraints of the circuit. It is important to note that the timing diagram should be adjusted to account for the specific timing requirements of the circuit design, such as rise/fall time and maximum input frequency.

4 Conclusion

Adder circuit were successfully implemented and verified using DSCH2. Truth tables and timing diagrams matched theoretical expectations, confirming correct logical and temporal behavior of each function.